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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,416	12/06/2001	Michael Ben Nun	Q65312	5429

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EXAMINER	
AHMED, SALMAN	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/003,416	NUN, MICHAEL BEN	
	Examiner	Art Unit	
	Salman Ahmed	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-50* is/are allowed.

6)☒ Claim(s) *1-8 and 11-16* is/are rejected.

7)☒ Claim(s) *9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because figure 1 and figure 2 should be labeled as "Prior Art". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 2 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Allan et al. (US PAT 5946313), hereinafter referred to as Allan.

In regards to claims 1, 2 and 11 applicant's disclosure of a network interface that processes data cells transmitted on a network operating in asynchronous transfer mode (ATM), comprising: a data path unit that inputs data cells transmitted on network; a header processor that inputs a first data cell from data path unit and determines

whether or not a full tuple can be created based on first data cell, wherein, if full tuple can be created based on first data cell, header processor constructs full tuple based on first data cell and outputs full tuple, wherein, if full tuple cannot be created based on first data cell, header processor inputs a second data cell of data cells from data path unit, constructs full tuple based on first data cell and second data cell, and outputs full tuple, wherein data path unit creates a data packet corresponding to full tuple is anticipated by the steps of sending Ethernet frame over atm. In column 6 lines 31-47 and figure 3B, Allan teaches that the payload field of the PDU is limited to 1,500 bytes, which is the size of the Ethernet payload field. To push PDU beyond Ethernet limit of 1,500 bytes will require an additional header in the Ethernet frame. The length of the header and trailer is between 6 and 40 bytes. Once the header and the trailer have been added to the user payload, the traffic is segmented into 44-48 bytes data units. Next, the adaptation layer adds a header, and possibly a trailer to the data unit, depending on the type of payload being supported. In any event, the final data unit from this operation is always a 48-octet block. Finally, the last operation is performed by the data link layer, which adds a five-octet header to the 48-octet payload resulting in a 53 bytes cell. In column 8 lines 29-41 Allan teaches frame manager receives the frame from interface, segments the frame and provides the payload to PDU manager, the VPI/VCI address to address processor and the type information to header processor. PDU manager generates a PDU by inserting the payload received from frame manager into field, and the type information from header processor into LLC/SNAP header field. PDU is then forwarded to SAR which segments the PDU into cells, for UNI 27. Address processor

inserts the VPI/VCI address from the source MAC ID field into each cell header, so that ATM network switches the cell accordingly.

In regards to claims 2 and 11, the classifier unit is anticipated by (column 9 lines 39-46) the steps of E-Mux receiving frame in step 240, and as the recipient, keeps the frame. It performs ATM AAL5 PDU and SAR processing on the payload steps 250 and 260, extracts the ATM virtual circuit address information from the frame source MAC and inserts it into the cells headers in step 270. The resulting cells are transmitted in step 280 over the address specified by the VPI/VCI address information.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4, 5, 6, 7, 8, 12, 13, 14, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allan and in view of Takiyasu et al. (US PAT 5113392).

In regards to claims 3, 4, 5, 6, 7, 8, 12, 13, 14, 15, 16 Allan teaches of segmenting Ethernet data packets into atm cells as described in the rejections of claim1 above.

In regards to claims 3 and 12 Allan does not teach a pointer memory that contains a pointer and a validity indicator, wherein pointer points to another memory location which stores information corresponding to at least a portion of full tuple and validity indicator identifies a characteristic of pointer. In regards to claims 5, 6, 7, 8, 15, 16 Allan does not teach the validity indicator corresponds to valid pointer data, pointer points to a first memory location when the valid pointer data has a first value and points to a second memory location when said valid pointer data has a second value. The first memory location contains information corresponding to first data cell. wherein first data cell is stored in first memory location and valid pointer data has first value when said full tuple cannot be created from said first data cell.

In regards to claim 3, 4, 5, 6, 7, 8, 12, 13, 14, 15, 16 Takiyasu teaches (column 2 lines 46-67 and column 3 lines 1-30) each communication apparatus (hereinafter simply called a node) stores, in a vacant memory block within a buffer memory, all data of each received cell or a part of the received cell which part is a field including a message information block (hereinafter called message information field). A next address pointer is stored in the memory block, the next address pointer pointing the address of a memory block stored in which are the data of a cell having the next information block of the same message in the message information field. The address indicating a vacant memory block within the buffer memory is stored beforehand, for example, in a first memory of a FIFO type. If a received cell is a cell containing the first information block of a message (FIRST cell) or a cell containing all information of a message (SINGLE

cell), the cell data are stored in a memory block identified by the address read from the first memory. It is not necessary to write a next address pointer in a memory block which stores the data of a SINGLE cell having no succeeding cell. Another address read from the first memory is written as the next address pointer in the memory block storing the FIRST cell data at the memory area following the cell data. There are also provided second to fourth memories. The second memory stores therein addresses used as next address pointers, correspondingly with each message. The third memory stores therein addresses indicating memory blocks which store FIRST cell data, correspondingly with each message. The fourth memory stores therein addresses indicating memory blocks, which store the first cell data of messages, which are allowed to be reassembled. The correspondence between cells and messages can be judged from a source node address contained in each cell. If a received cell is a cell containing the last information block of a message (LAST cell) or a cell containing an intermediate information block between the first and last information blocks (LAST cell), the cell data are stored in a memory block identified by an address pointer read from the second memory. If a received cell is a NEXT cell, in the similar manner as the FIRST cell, an address read from the first memory is stored as the next address pointer in the memory block and in the second memory. If a received cell is a LAST cell, in the similar manner as the FIRST cell, it is not necessary to store the next address pointer in the memory block and in the second memory. If a LAST cell is received, the address indicating the memory block storing the cell data of the corresponding FIRST cell is transferred from the third memory to the fourth memory. In column 11 lines 4-11, Takiyasu teaches, in

order to discriminate the SINGLE cell and LAST cell from other cells (such as FIRST cell, NEXT cell) during the read cycle, a zero address is written in the next address pointer field of a memory block storing a SINGLE cell or LAST cell.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Allan's teaching by incorporating Takiyasu's teaching of using memory buffers and pointers while packet segmentation and reassembly. The motivation is as suggested by Takiyasu (column 2 lines 32-36) such arrangement would provide a communication apparatus capable of efficiently using a buffer memory for storing received packets and reassembling them without discarding any received packets because of insufficient memory area.

Allowable Subject Matter

5. Claims 9 and 10 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. Claims 17-50 are allowed.

Reason for Allowance

7. The following is an examiner's statement of reasons for allowance: The instant application claims a method and software for classifying internet protocol (1P) packets

transferred in data cells over an asynchronous transfer mode (ATM) network, comprising: determining if a first data cell contains a full IP tuple; creating full IP tuple from first data cell if first data cell contains full IP tuple; classifying full IP tuple in accordance with process flow information after full IP tuple is created; determining a first pointer based on a virtual channel identifier/virtual path identifier (VCI/VPI) contained in first data cell; storing a second pointer and validity data in a first memory location, wherein first pointer points to first memory location; storing process flow information in a second memory location, wherein second pointer points to second memory location after said full IP tuple is created; obtaining an IP packet corresponding to full IP tuple; and determining operations to be performed on said IP packet based on said process flow information.

8. The prior arts alone or in combination fail to jointly suggest or teach the claimed combination of features as taught by the instant application. The prior arts do not specifically teach a method and software for classifying internet protocol (1P) packets transferred in data cells over an asynchronous transfer mode (ATM) network, comprising: determining if a first data cell contains a full IP tuple; creating full IP tuple from first data cell if first data cell contains full IP tuple; classifying full IP tuple in accordance with process flow information after full IP tuple is created; determining a first pointer based on a virtual channel identifier/virtual path identifier (VCI/VPI) contained in first data cell; storing a second pointer and validity data in a first memory location, wherein first pointer points to first memory location; storing process flow information in a

second memory location, wherein second pointer points to second memory location after said full IP tuple is created; obtaining an IP packet corresponding to full IP tuple; and determining operations to be performed on said IP packet based on said process flow information.

Citation of Relevant Prior Art

9. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

10. The cited prior art Gaddis et al. (US PAT 5457681), hereinafter referred to as Gaddis, teaches an ATM-Ethernet portal/concentrator permitting a transparent interconnection between Ethernet segments over an ATM network to provide remote connectivity for Ethernet segments. The portal includes an Ethernet controller and an ATM cell processor, both of which receive and transmit data to and from a dual port shared memory under control of a direct memory access controller. A control microprocessor monitors and controls the shifting of data through the dual port memory. In this scheme, original data is written and read directly into and out of the dual port memory to thereby eliminate any requirement for copying of data, to thereby significantly increase the data throughput capability of the portal. In the concentrator embodiment, a plurality of Ethernet controllers, each of which is connected to its own associated Ethernet segment, is multiplexed through the concentrator to an ATM network to thereby provide remote connectivity for each of the Ethernet segments.

11. The cited prior art Kudoh (US PAT 5414702) teaches a packet disassembler, which eliminates the need of an upper-level processor to have an excessive processing ability, includes a plurality of fixed-length buffers having a storage capacity corresponding to a multiple of the byte length of an information field of input packets having a predetermined fixed length and each of the fixed-length buffers has an identical length. Also included in the packet disassembler is manager which, when disassembling ones of the input packets having an identical connection identifier within their headers or having a multiplexing identifier on the same connection is not completed, performs allocation control of associating the packets having the identical identifier with one of the plurality of fixed-length buffers having the identical identifier, and when the disassembling of the packets having the identical identifier is completed or when no disassembling of the packets having the identical identifier is carried out, performs allocation control of associating the associated packets with an empty one of the plurality of fixed-length buffers.

12. The cited prior art Mesh et al. (US PAT PUB 2002/0085563), hereinafter referred to as Mesh, teaches a method for packet processing for data transmission over an optical fiber, the method including the steps of segmenting an incoming bit stream, adding a tag to a header of each segment, each tag including data identifying a route between a source and a destination end-point of the bit stream, encapsulating the

tagged segment into a Point-to-Point Protocol (PPP) packet, and mapping the encapsulated packet into a transmission frame (SONET/SDH or other) for transmission over an optical fiber.

13. The cited prior art Assa et al. (US PAT PUB 2004/0213222), hereinafter referred to as Assa, teaches an Electronic device including Asynchronous Transfer Mode (ATM) switching capabilities or including interior fixed length packet/cell processing for use in telecommunication networks. The electronic device includes a buffer of incoming cells of packets, the cells are assigned, each within Virtual Path Identifier (VPI) and Virtual Channel Identifier (VCI), such that all cells of the same packet bear the same VCI. Each VCI is associated with data that include data item serving for packet efficiency mechanism. The device further includes storage medium storing data representative of data structure for storing selected number from the specified data items. The device further includes processor associated with the storage medium that is configured to perform the processing procedures that include: for each incoming cell whose VCI is associated with data item that is stored in the data structure constructing a search key that enables to access said data item at substantially O(1).

14. A 1995 publication *High speed datagram delivery over internet using ATM technology* by Esaki et al teach how to carry TCP/IP over ATM, or, in general, how to carry connectionless and/or connection oriented network layer protocol over connection oriented QoS-ed datalink layer. Low latency property of ATM is fully extracted both for

connectionless and connection oriented communication over TCP/IP without changing the current architecture of TCP/IP network.

A 1998 publication *IP Switching: ATM Under IP* by Newman et al teach discarding the end-to-end ATM connection and integrate fast ATM hardware directly with IP, preserving the connectionless nature of IP. Usage of Soft-state in the ATM hardware to cache the IP forwarding decision. This enables further traffic on the same IP flow to be switched by the ATM hardware rather than forwarded by the ATM hardware rather than the IP software.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571)272-8307. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571)272-3174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Salman Ahmed
Examiner
Art Unit 2666

SA
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DANG TON
PRIMARY EXAMINER